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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,030	12/11/2001	Philip David Steiner	026-0013	6289

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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,030	STEINER ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-37 and 39-43* is/are rejected.

7)☒ Claim(s) *17 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Specification

2. The disclosure is objected to because of the following informalities: page 5, line 8, "register 116" should be "register 115"; page 17, line 16, "multiplexer 103" should be "multiplexer 107"; page 15, line 28, "Fig. 10" should be "Fig. 9". Appropriate correction is required.

Allowable Subject Matter

3. The indicated allowability of claims 1-43 is withdrawn in view of the newly discovered reference(s) to Loinaz et al. and Coffey et al.. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-10, 14-16, 18-35, 37 and 39-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Loinaz et al. (US 6,377,082 B1 herein after "Loinaz").

Loinaz discloses a loss-of-signal (LOS) detector circuit in Figure 3 for use in a clock and data recovery circuit shown in Figure 1. In Figure 3, the LOS detector circuit comprises a transition detector 301 and an inconsistency detector 303 for detecting data bits of an input data 102 with decision thresholds to a logic circuit 315 for generating LOS indication.

With respect to claims 1, 28-31 and 42-43, the operation of comparing signal strength of the plurality of data bits of the input data stream 102 to a signal strength threshold level to generate an indication thereof and determining a count value according to the indication can be performed either by the transition detector 301 (see column 2, lines 9-20) or the inconsistency detector 303 (see column 4, line 35 to column 5, line 11); the operation of generating the LOS indication according to the count value is performed by the logic circuit 315.

With respect to claims 2-3, 14 and 39, the operation of sampling the input data stream 102 is performed by the D Flip-Flops or counters 312. Although Loinaz does not explicitly show or suggest that the sampling rate of the recovered clock 128 from the voltage controlled oscillator (VCO) 126 of the clock and data recovery circuit of Figure 1 is below or higher than the data rate of the input data stream 102, it is well known to a person skill in the art to recognize that the frequency of the VOC 126 within a phase

locked loop (PLL) circuit is sometimes frequency divided/multiplied by an integer value of a divider/multiplier for frequency integrating/interpolating the sampling rate of the oscillation frequency.

With respect to claims 4 and 18, the LOS indication 136 is compared by the logic circuit 135 between the count value generated by the counter 321 and a threshold count, which is generated by the transition detector 301.

With respect to claims 5, 23 and 40-41, although Loinaz does not explicitly show or suggest that the threshold count is programmable, it is the choice of design to determine whether the threshold count is a fixed threshold count or programmable by other devices.

With respect to claims 6-8 and 32-34, the threshold count is variable or increases when the LOS indication is asserted because the transition detector 301 detects transitions in a specified time period.

With respect to claims 9-10, the logic circuit 317 latches a first value in the register 312 when the signal strength of a data bit of the input data stream 102 is above the signal strength threshold level 304 (main) and latches a second value in the register 312 when the signal strength of the data bit 102 is below the signal strength threshold level 304 (Aux), wherein the amplifiers 308 provide the amplification signals to the registers 312.

With respect to claims 15-16 and 37, the logic circuit 317 is coupled to the registers 312 and provides a count control signal to the counter 321 to determine the count value having signal strength above or below the decision threshold 304.

With respect to claims 19-22 and 24-26, the transition detector 301 (or 201 shown in Figure 2) detects a stuck-at-one or a stuck-at-zero condition. The transition detector 301 is a logic circuit that samples the input data signal 102 using the recovered clock signal 128 and counts the number of 0-to-1 and 1-to-0 transitions occurred in a specified time period. See column 2, lines 9-16. Although Loinaz does not explicitly show or suggest that the comparing is performed for each of four phases of a clock before a decision is made that the LOS condition exists, it is inherent and well known to a person skill in the art to know that the recovered clock 128 is controlled the VCO circuit 126 of the PLL circuit in Figure 1, wherein the phase detector 120 of the PLL circuit detects the incoming frequency and the feedback frequency a certain period of time until the phases are locked in order generate to a recovered clock signal.

With respect to claim 27, the decision threshold(s) is defined by an analog signal on an input terminal of the amplifiers 308.

With respect to claim 35, wherein the sampling circuits 306 include amplifiers 308 for amplifying the input data stream 102 and the offset of the main and auxiliary decision thresholds.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 11-13 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loinaz et al. as applied to claims 1, 9-10 and 30 above in view of Coffey et al. (US 6,492,929 B1 herein after "Coffey").

Loinaz fails to show or suggest that the offset of the decision thresholds 304 supplied to the amplifiers 308 comprises a first portion of a digital value indicative of the offset is supplied to a first DAC and a second portion of the digital value is supplied to a second DAC, the offset being formed from outputs of the first and second DACS, wherein at least a portion of the value supplied to the first and second DACS overlap, as recited in claims 11-13 and 36.

Coffey discloses a signal comparison and level change detection circuit in Figure 5 comprising two comparators or amplifiers 20 and 22 for comparing an input signal with an upper threshold value and a lower threshold value, respectively to generate a time interval or a timing recovery signal to time circuitry at stage 4 of Figure 3 via a threshold transition and direction logic circuit at stage 3. As shown in Figure 5, a first portion of a

digital count value outputted from the counter 28 is supplied to a first D-to-A converter 24 to generate the upper threshold lever and a second portion of the digital count value is supplied to a second D-to-A converter 26 to generate the lower threshold level to the comparators 20 and 22,respectively, wherein at least a portion of the count value supplied to the first and second D-to-A converters overlap.

Therefore, it would have been obvious to one of ordinary skill in the art to include two digital to analog converters internal or external to Loinaz's inconsistency detector 303 for converting a digital value into two analog threshold levels as taught by Coffey in order to generate an offset of the upper and lower threshold levels to the comparators or amplifiers 308 for generating timing recovery clock signals prior the determination of the LOS indication.

Allowable Subject Matter

9. Claims 17 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to show or suggest that a decimator circuit comprises a one-to-transition converter, a divide by n circuit, and a transition-to-one converter is coupled between a sampling circuit for sampling the signal strength of a data bit of an input data stream above a signal strength threshold level and the signal strength of the data bit of the input data stream below the signal strength threshold level and a counter for

generating a count value used to generate a loss-of-signal indication for the input data stream.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The Central FAX Number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE
Primary Examiner
Art Unit 2637